



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of : Prashanth Bhat et al.

Examiner: Shah, Nilesh R.

Application No. : 09/865,988

Group Art Unit: 2127

Filing Date : May 25, 2001

Art Unit : 2127

Title : LOAD BALANCING SYSTEM AND METHOD IN A
MULTIPROCESSOR SYSTEM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**NOTICE OF APPEAL FROM THE PRIMARY EXAMINER
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Sir:

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the Office Action dated April 15, 2005 of the Primary Examiner finally rejecting claims 1-39 of the above-referenced patent application.

Enclosed is a check in the amount of \$1520.00, which includes the \$500.00 Notice of Appeal fee.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or to credit any overpayment to Deposit Account No. 02-4270.

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Dated: 10/14/05

I hereby certify that the correspondence attached herewith is being transmitted by First Class Mail to, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450:

Kim Dufault
Kim Dufault

10-14-05
Date

Respectively submitted,

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